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2       What is claimed is:

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4       1. A symbol timing synchronizer for generating a timing signal from  
5 a sampled input signal being a received input signal sampled at a  
6 rate of the timing signal, the received input signal being a  
7 continuous phase modulated signal modulated by a symbol sequence  
8 generated from a precoded data sequence of an input data sequence,  
9 sampled input signal having a sampled inphase component and a  
10 sampled quadrature component, the symbol timing synchronizer  
11 comprising,

12       an inphase isolator and a quadrature isolator for respectively  
13 isolating the sampled inphase component and sampled quadrature  
14 component of the sampled input signal for respectively providing an  
15 inphase signal and a quadrature signal,

16       an inphase serial data demodulator and a quadrature serial  
17 data demodulator for respectively receiving and filtering the  
18 inphase signal and the quadrature signal for generating an odd  
19 filter response and an even filter response, and for converting and  
20 sampling the odd and even filter responses into odd data and even  
21 data, the odd data and the even data alternately forming an  
22 estimate of the input data sequence,

23       an inphase error magnitude generator and a quadrature error  
24 magnitude generator for receiving and filtering the inphase signal  
25 and the quadrature signal, for respectively generating and sampling  
26 an inphase error magnitude signal and quadrature error magnitude  
27 signal for respectively generating a sampled inphase error  
28 magnitude signal and a sampled quadrature error magnitude signal,

1 an inphase mixer and a quadrature mixer for respectively  
2 mixing the sampled inphase error magnitude signal with the odd data  
3 into an odd error signal, and mixing the quadrature error magnitude  
4 signal with the even data for generating an even error signal, the  
5 odd data representing an odd sign of the inphase magnitude error  
6 signal, the even data representing an even sign of the quadrature  
7 magnitude signal, and

8 an oscillator means for generating the timing signal from the  
9 even error signal and the odd error signal, the timing signal for  
10 controlling the sampling of the inphase serial data demodulator and  
11 the quadrature serial data demodulator and for controlling the  
12 sampling of inphase error magnitude generator and a quadrature  
13 error magnitude generator for generating the timing signal at a  
14 rate of the symbol sequence.

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18 2. The symbol timing synchronizer of claim 1 wherein the oscillator  
19 means comprises,

20 a loop filter for receiving the odd error signal and the even  
21 error signal for providing a filter error signal,

22 a controlled oscillator for receiving the filter error signal  
23 for generating the timing signal, and

24 a modulo counter for providing an odd timing signal for  
25 sampling the inphase magnitude error signal, and for providing an  
26 even timing signal for sampling the quadrature magnitude error  
27 signal.

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1 3. The symbol timing synchronizer of claim 1 wherein,  
2 the inphase magnitude error generator generates the inphase  
3 magnitude error signal from a difference between a filter response  
4 of the inphase signal and an odd modulo count of the timing signal,  
5 the inphase magnitude error generator serving to cross correlate a  
6 principal Laurent component of the inphase signal with a gate  
7 function relative to the odd modulo count of the timing signal, and  
8 the quadrature magnitude error generator generates the  
9 quadrature magnitude error signal from a difference between a  
10 filter response of the quadrature signal and an even modulo count  
11 of the timing signal, the quadrature magnitude error generator  
12 serving to cross correlate a principal Laurent component of the  
13 inphase signal with a gate function relative to the even modulo  
14 count of the timing signal.

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17 4. The symbol timing synchronizer for claim 1 wherein,  
18 inphase and quadrature serial demodulators respectively filter  
19 principal Laurent components of the inphase and quadrature signals  
20 for providing odd and even Laurent filter responses, and

21 inphase and quadrature serial demodulators respectively  
22 sample the odd and even Laurent filter responses for generating the  
23 odd and even data.

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26 5. The symbol timing synchronizer of claim 1 further comprising  
27 an input sampler for sampling the received signal into the  
28 sampled input signal sampled at a rate of the timing signal.

- 1 6. The symbol timing synchronizer of the claim 1 further  
2 comprising,  
3 a multiplexer for multiplexing the odd and even data into the  
4 estimate of the input data sequence.  
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- 6 7. the symbol timing synchronizer of claim 1 wherein,  
7 the received input system is a Gaussian minimum shift keying  
8 signal have a bit bandwidth product of  $1/5$  and a modulation index  
9 of  $1/2$ .  
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- 11 8. The symbol timing synchronizer of claim 3 wherein,  
12 the odd modulo count is  $(2k+1)N$  where  $N$  is the modulo count of  
13 the modulo counter, and  
14 the even modulo count is  $(2k)N$  where  $N$  is the modulo count of  
15 the modulo counter  
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- 17 9. The symbol timing synchronizer of claim 1 wherein  
18 the odd error signal is an  $e_{2k+1}$  odd error signal, and  
19 the even error signal is an  $e_{2k}$  even error signal.  
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- 21 10. The symbol timing synchronizer of claim 1 further comprising  
22 a carrier phase synchronizer for generating a phase adjustment  
23 signal from a sampled phase adjusted input signal and the timing  
24 signal,  
25 an input mixer for adjusting the received input signal into a  
26 phase adjusted input signal, and  
27 an input sampler for sampling the phase adjusted input signal  
28 into the sampled phase adjusted input signal.

1 11. The symbol timing synchronizer of claim 10 wherein the carrier  
2 phase synchronizer comprises,  
3 an inphase isolator and a quadrature isolator for respectively  
4 isolating the sampled inphase component and sampled quadrature  
5 component for providing an inphase signal and a quadrature signal,  
6 an inphase serial data demodulator and a quadrature serial  
7 data demodulator for respectively receiving and filtering the  
8 inphase signal and the quadrature signal for generating an odd  
9 filter response and an even filter response, and for converting and  
10 sampling the odd and even filter responses into odd data and even  
11 data, the odd data and the even data alternately forming an  
12 estimate of the input data sequence,  
13 an odd mixer and an even mixer for respectively mixing the  
14 even filter response and the odd data signal into an odd error  
15 signal and mixing the odd filter response signal and the even data  
16 signal into an even error signal, and  
17 an oscillator means for converting the odd and even error  
18 signals into the phase adjustment signal.

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12. A symbol timing synchronizer for generating a timing signal from a sampled input signal being a received input signal sampled at a rate of the timing signal, the received input signal being a continuous phase modulated signal modulated by a symbol sequence generated from a precoded data sequence of an input data sequence, sampled input signal having a sampled inphase component and a sampled quadrature component, the symbol timing synchronizer comprising,

an inphase isolator and a quadrature isolator for respectively isolating the sampled inphase component and sampled quadrature component of the sampled input signal for respectively providing an inphase signal and a quadrature signal,

an inphase early-late gate and a quadrature early-late gate for respectively filtering the inphase signal and the quadrature signal for generating an inphase gate signal and a quadrature gate signal, the inphase and quadrature early-late gates respectively serving to cross correlate the inphase and quadrature signals with gate functions in synchronism with the timing signal,

an inphase transformer and a quadrature transformer for respectively transforming the inphase signal and the quadrature signal for generating an inphase transformed signal and a quadrature transformed signal,

an inphase gate sampler and a quadrature gate sampler for respectively sampling inphase gate signal and the quadrature gate signal for generating a sampled inphase gate signal and a sampled quadrature gate signal,

1 an inphase transformer sampler and a quadrature transformer  
2 sampler for respectively sampling the inphase transformed signal  
3 and the quadrature transformed signal for generating a sampled  
4 inphase transformed signal and a sampled quadrature transformed  
5 signal,

6 an inphase hard limiter and a quadrature hard limiter for  
7 respectively converting the sampled inphase transformed signal into  
8 odd data and the sampled quadrature transformed signal into even  
9 data,

10 an inphase mixer and a quadrature mixer for respectively  
11 mixing the sampled inphase gate signal and odd data into an odd  
12 error signal and mixing the sampled quadrature gate signal and even  
13 data signal into an even error signal, and

14 an oscillator means for generating the timing signal from the  
15 even error signal and the odd error signal, the oscillator means  
16 for controlling the sampling of the inphase and quadrature gate  
17 samplers and the inphase and quadrature transformer samplers for  
18 generating the timing signal at a rate of the symbol sequence.

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1 13. The symbol timing synchronizer of claim 12 wherein the  
2 oscillator means comprises,

3 a loop filter for receiving the odd error signal and the even  
4 error signal for providing a filter error signal,

5 a controlled oscillator for receiving the filter error signal  
6 for generating the timing signal, and

7 a modulo counter for providing an odd timing signal for  
8 sampling the inphase magnitude error signal, and for providing an  
9 even timing signal for sampling the quadrature magnitude error  
10 signal.

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13 14. The symbol timing synchronizer of claim 12 wherein,

14 the inphase and quadrature early-late gates function as cross  
15 correlators for cross correlating a filter response isolating  
16 principal Laurent components of the inphase and quadrature signals  
17 with a gating function,

18 the inphase gate signal is an inphase magnitude error signal  
19 from the correlation of an inphase early-late gate filter response  
20 of the inphase signal and the gating function that is in  
21 synchronism with an odd modulo count of the timing signal, and

22 the quadrature gate signal is a quadrature magnitude error  
23 signal from the correlation of a quadrature early-late gate filter  
24 response of the quadrature signal and the gating function that is  
25 in synchronism an even modulo count of the timing signal.

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1 15. The symbol timing synchronizer for claim 12 wherein,  
2 the inphase and quadrature transformers, transformer samplers  
3 and hard-limiters respectively are inphase and quadrature serial  
4 demodulators,  
5 the inphase and quadrature transformer are principal Laurent  
6 component filters providing the inphase and quadrature transformed  
7 signals that respectively are odd and even Laurent filter  
8 responses, and  
9 the odd and even data alternately forming an estimate of the  
10 input data sequence.

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12 16. The symbol timing synchronizer of claim 12 further comprising  
13 an input sampler for sampling the received signal into the  
14 sampled input signal sampled at a rate of the timing signal, and  
15 a multiplexer for multiplexing the odd and even data into the  
16 estimate of the input data sequence.

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19 17. The symbol timing synchronizer of claim 12 wherein,  
20 the received input system is a Gaussian minimum shift keying  
21 signal have a bit bandwidth product of  $1/5$  and a modulation index  
22 of  $1/2$ ,  
23 the odd modulo count is  $(2k+1)N$  where  $N$  is the modulo count of  
24 the modulo counter,  
25 the even modulo count is  $(2k)N$  where  $N$  is the modulo count of  
26 the modulo counter,  
27 the odd error signal is an  $e_{2k+1}$  odd error signal, and  
28 the even error signal is an  $e_{2k}$  even error signal.

1 18. The symbol timing synchronizer of claim 12 further comprising  
2 a carrier phase synchronizer for generating a phase adjustment  
3 signal from a sampled phase adjusted input signal and the timing  
4 signal,

5 an input mixer for adjusting the received input signal into a  
6 phase adjusted input signal, and

7 an input sampler for sampling the phase adjusted input signal  
8 into the sampled phase adjusted input signal.

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10 19. The symbol timing synchronizer of claim 18 wherein the carrier  
11 phase synchronizer comprises,

12 a carrier inphase isolator and a carrier quadrature isolator  
13 for respectively isolating the carrier sampled inphase component  
14 and carrier sampled quadrature component for providing a carrier  
15 inphase signal and a carrier quadrature signal,

16 an inphase sampler and a quadrature sampler for respectively  
17 sampling at the rate of the timing signal the carrier inphase  
18 signal and the carrier quadrature signal for providing a carrier  
19 sampled inphase signal and a carrier sampled quadrature signal,

20 a carrier inphase transformer and a carrier quadrature  
21 transformer for respectively transforming the carrier sampled  
22 inphase signal and carrier sampled quadrature signal into a carrier  
23 inphase transformed signal and a carrier quadrature transformed  
24 signal,

25 a carrier inphase hard limiter and a carrier quadrature hard  
26 limiter for respectively converting the carrier inphase transformed  
27 signal and carrier quadrature transformed signal into a carrier odd  
28 hard limited signal and a carrier even hard limited signal,

1 a carrier modulo counter for receiving the timing signal and  
2 generating a carrier odd timing signal and a carrier even timing  
3 signal,  
4 a carrier odd sampler and a carrier even sampler for  
5 respectively sampling at the rate of the carrier odd and even  
6 timing signals for sampling the carrier odd and even hard limited  
7 signals into carrier odd data and carrier even data,  
8 a carrier odd mixer and a carrier even mixer for respecting  
9 mixing the carrier quadrature transformed signal and the carrier  
10 odd data signal into a carrier odd error signal and the carrier  
11 inphase transformed signal and the carrier even data signal into a  
12 carrier even error signal, and  
13 a carrier oscillator for converting the carrier odd and even  
14 error signals into the phase adjustment signal.

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